

## Strategic Partnerships

For semiconductor companies world over, the need for high-competence, resource-rich, customer-focused strategic partners can never be over emphasized. With huge investments riding on cutting edge chip design solutions, with extreme pressures on go-to-market deadlines, they need relationships that can stand up to the challenges and deliver, on time. Discover Kacper, the right partner for strategic relationships, for all the right reasons.

## About Kacper

Kacper is a semiconductor organization that is focused on providing complete solutions in Architecture, Design, Synthesis, and Verification of SoC/ASIC/FPGA/IP's. We are able to deliver the best-in-class solutions through a motivated team of VLSI engineers, who have the expertise in:

- Hardware Description Languages like Verilog, VHDL and SystemVerilog.
- Hardware Verification Languages: SystemVerilog.
- Verification Frameworks: VMM,OVM,UVM and VMM\_LP.
- Domain expertise in SONET /SDH, Next generation SONET/SDH, OTN, 10GbE,CAN , FlexRay, RISC Processors, AMBA-AXI series and AMBA AHB series.
- Development of test benches, test vectors, test automation tools using SystemVerilog and scripting languages like Perl, C-Shell and TCL.
- Verification Technologies: Constrained Random Stimulus Generation, Assertion Based Verification and Coverage Driven Verification
- Using the latest tools and methodologies

## Kacper's Focus Areas

Kacper Technologies believes in the power of focus. Consequently, our engineers have specialized in providing solutions for customers in Telecom, Processors, Peripherals, Automotive Protocols, Interconnects, 3<sup>rd</sup> Party IP Integration and Reuse.

## Flexible Engagement Model

Kacper Technology partners with customers through various modes of engagement on different levels – in terms of taking responsibility for a customer's R&D requirements, location of the team and pricing model chosen. Our different working models give our customers the flexibility of choosing how they would like to work with us.

### Complete Product Development

In this model of engagement, Kacper takes complete responsibility of customer's product(s) from concept-to-

market. This helps customers to focus on conceptualizing next-generation products.

### Modular Development

This happens when customers outsource the development of bits and pieces of their product(s) to Kacper. Product integration skills to put together these modules become a key aspect for both the customer and Kacper.

### Co-Development

This is a model where the customer and Kacper work in a coordinated manner to develop a product . Kacper's team is considered an extension of the customer' team and has all the rights and privileges to work on the customer's code base.

### Specific Services

Here, customers outsource certain activities of the product lifecycle, such as testing, documentation or product implementation, but not the core development activity itself. Another key advantage of this model is that the source code of the product does not have to be shared with Kacper to begin working together.

## Location

### Pure Offshore

In this model the development effort fully happens in Kacper's offshore development Center at Bangalore and the customer takes care of project management. This works out to be the most cost effective working model, in terms of location, for the customer.

### Onsite /Offshore

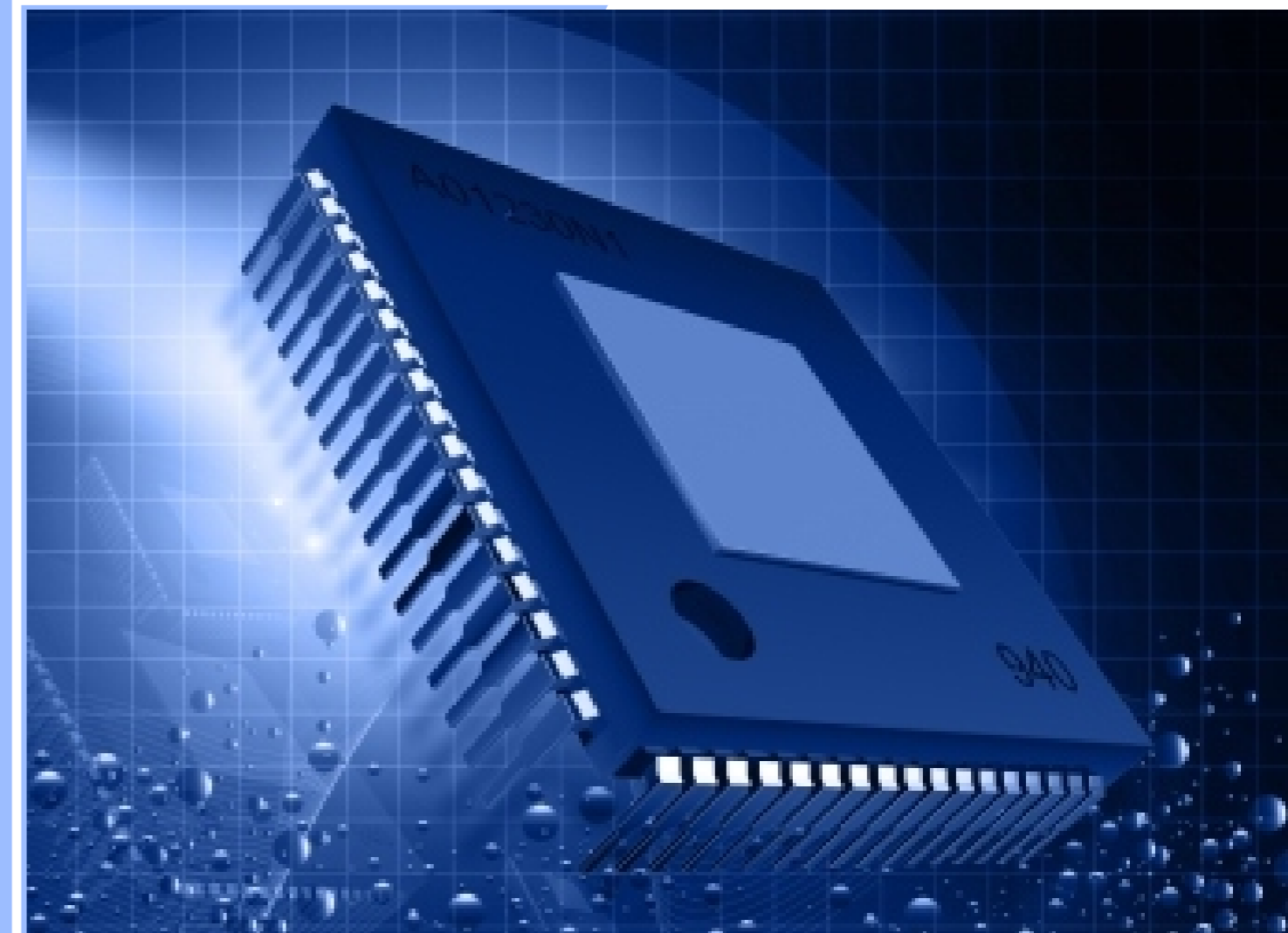
Kacper's onsite/offshore model provides customers the satisfaction of co-ordinating and discussing requirements and deliverables with an onsite Kacper team, while enjoying the benefits of offshore outsourcing. This is the preferred model when the client wants to achieve more within his budget and the project requirements are better understood.

## Why Kacper?

Some reasons why Kacper's semiconductor solutions are the right choice for your organization:

- Domain expertise: We have a good understanding of our specialization areas.
- Proven track record: We have sustained relationships with organizations of all sizes, because of our successful solutions, delivered on time.
- Flexibility: Kacper gives you unmatched flexibility.
- Start small, grow big: Kacper understands the concerns of global corporations. We believe in growing relationships through creating successful proof of concept.
- Long-term support: Kacper is committed to providing strategic support to all its customers.

**KACPER**  
designing future



For more information, please call us or write to [sales@kacpertech.com](mailto:sales@kacpertech.com)

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designing future

**Design & Verification for  
SoC/ ASIC/FPGA/IP**

**VLSI**  
Solutions

Kacper's VLSI (ASIC & FPGA) design team has the capabilities to handle complex multimillion gate designs.

**Our Offerings:**

- Generation of system specification requirements
- Defining Partition of hardware-software
- Definition of high-level architecture
- Definition of micro-architecture
- Development and verification of reference model
- Analysis of performance/trade-off
- RTL Coding
- Evaluation, customization and integration of IP if required

**Key Benefits:**

- Lower rate of failure or re-spin. Reduced time to market.
- Remarkable improvement in development productivity.
- Cost effective.

**Our Deliverables:**

- Design documents.
- RTL source code.
- Synthesis scripts.
- Test benches and Test suites.

Kacper enables you to rapidly build verification environments there by helping you to achieve your design and verification targets through our unique blend of innovative tools and technologies.

**Features:**

- Our verification methodology helps to build highly layered, scalable, reusable and extensible verification environments for module and SoC/ASIC/FPGA/IP level verification, providing maximum functional coverage.
- We are well equipped to provide proven and innovative solutions
- We provide complete verification solutions - right from verification plan to silicon tape-out.

**Capabilities:**

- Development of Verification plan.
- Development of reusable verification environment at module, chip or SoC level using Verification methodologies like VMM, OVM, UVM and VMM\_LP.
- Development of Self-Checking Test cases and Regression suites.
- Development of Assertion Based Checkers and Protocol Monitors.
- Functional and Code Coverage Analysis.
- Test case execution and analysis.
- Verification report generation

**Deliverables:**

- Verification Plan.
- Verification Report.
- Test Benches and Test Suites.
- Support Scripts.
- Verification IP's.

**Our services include:**

- Language testing (LRM compliance)
- Low Power Simulation with test cases on Retention, Isolation and LS
- Methodology compliance
- Functional tests for release qualification
- Reconciliation of Migration issues
- GUI testing
- Performance testing
- Development of Regression Environments
- Identification of Bugs and Enhancements

**Expertise Areas:**

- SystemVerilog compilers, simulators
- Interoperability of various methodologies on compilers and simulators
- VHDL/Verilog mixed simulations
- Tool Validation for Assertions and Coverage .
- Tools Validation for Low Power Design and Verification

**Our Deliverables:**

- Test Plans
- Test Suites for Regression
- Automated Test benches
- Documentation with bug list and enhancements



Design Services

Products - Design IP

Products - Verification IP

EDA Validation Services

**SONET /SDH Design IP**

SONET/SDH has become the worldwide standard for interface and multiplexing of user information to optical networks. SONET/SDH systems allow much greater network flexibility and management over existing optical systems. Kacper provides framing, pointer processing and overhead processing solutions.

**Features:**

- Compliant with SONET GR-253-CORE and SDH ITU-T G.707.
- The framer supports standard SONET mappings down to OC-48 channels and can be used either as a single OC-48 framer or 4 individual OC-12 framers.
- Provides access to internal registers through a Control Interface.
- Performs Byte & Frame Alignment on the Receive Signal.
- Pointer Processors at STS/STM and VT/TU levels.
- Generates Frame Co-ordinates (N, row, column) for path processing.
- Accepts external synchronization pulse for the transmit start of frame.
- Inserts the Framing Bytes (A1, A2) and Section Trace J0 Byte or STS-1 ID(C1).
- Optionally inserts the section and line data communication channels (D1-D3) or (D4 – D12).
- Optionally inserts register programmable APS Byte failure (K1, K2) and synchronization status S1 Bytes.
- Computes and inserts section BIP-8 (B1), line BIP-8 (B2), path BIP-8 (B3)and Path Far End Block Error FEBE (G1).
- Optionally scrambles the Transmit Frame data and optionally descrambles the receive frame data.
- Remote defect, error and failure indications (AIS-L, AIS-P, AIS-V, MS-AIS, AUAIS,TU-AIS).
- Pass through of TOH bytes.
- Supports 16-bit asynchronous and synchronous microprocessor interface up to OC- 48.
- Fully synthesizable Register Transfer Level (RTL) Verilog/VHDL Core.

**Next Generation SONET/SDH**

- NG-SONET/SDH IP is a comprehensive solution for pre-silicon functional verification of NG-SONET/SDH designs.
- It is developed using SystemVerilog and adheres to VMM, OVM and UVM.
- VMM\_LP compliant with in built assertion based checkers for Low Power simulation
- It is a highly reliable and configurable solution available for the verification of Next Generation SONET/SDH systems
- Includes Extensive test suite that allows design and verification engineers to quickly and extensively test the entire functionality of their NG -SONET/SDH compliant designs.
- Compliance to Bellcore GR-253, ITU G.707, G.7041 and G.7042.
- Re-usable Verification IP, Scalable and Modular.
- Predefined cover points defining functional coverage.
- Constraint Random Verification along with a choice of driving directed test cases.
- Well defined Scenario Layer for configuring scenarios with frame control
- Efficient error insertion mechanism.
- Assertion based checkers for checking the functionality of pointer processor, framer and alarms.
- Simple hookup and interaction without any special interfaces.
- Ability to interact with various design languages.
- Completely Configurable at all levels of SONET/ SDH up to STS-192/STM-64.
- SDH/ SONET overhead control and decode.
- Alarm and Error Insertion capabilities.
- Efficient error insertion mechanism for B1,B2,B3 and pointers
- Configurable to cover all kinds of pointer adjustments (STS/ STM and VT/ TU Level).
- Provisioning Capabilities for all levels
- Supports all valid sizes and combinations of contiguous concatenation
- Fully supports Telcordia GR253/2000 Table 5.1 and ITU-T G.707 for payload concatenation

**GFP ( Generic Framing Procedure)**

- System level capability of end-to-end frame delineation.
- Support for both client management and data frames.
- Ethernet frames generation via GFP-F and GFP-T.

**VCAT (Virtual Concatenation)**

- VCAT Path overhead bytes control and decode on each member.
- VCAT Error Injection or Alarm Generation on each member

**LCAS (Link Capacity Adjustment Scheme)**

- Emulation of Source and Sink State Machines (per member).
- Generation and capture of member status information.
- Capability to ADD ,DELETE and DNU a member in the VCAT Group

**10 Gigabit Ethernet**

- The accelerating growth of worldwide network traffic is forcing service providers, enterprise network managers and architects to look to ever higher speed network technologies in order to solve the bandwidth demand crunch. Kacper has developed 10 Gigabit Ethernet Verification IP in VMM/OVM/UVM to test the entire functionality of 10 Gigabit Ethernet DUT.
- Quickly validates interpretation and implementation of the Gigabit and 10 Gigabit Ethernet standards.
  - Constantly monitors Gigabit and 10 Gigabit Ethernet behaviors during simulation.
  - Enables rapid application of static and dynamic formal verification to validate interface designs.
  - Emulation of Source and Sink State Machines (per member).
  - Constantly monitors Gigabit and 10 Gigabit Ethernet behaviors during simulation.
  - Generation and capture of member status information.
  - Measures structural coverage to grade test bench efficiency across multiple simulations and formal verification.
  - Errors, statistics, and corner cases can be analyzed in assertion management environment.